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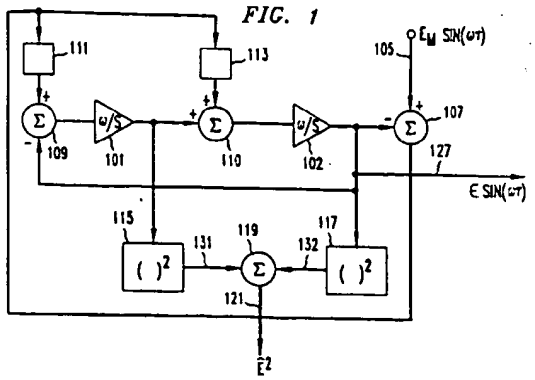
## (54) Circuit for estimating a peak or RMS value of a sinusoidal voltage waveform.

(57) An estimating circuit for application in estimating or deriving the value $V^2_{rms}$ or $V^2_{peak}$, of a line voltage $V_{AC}$ provides fast response time and a substantially ripple free value for these signals by the utilization of a controlled harmonic oscillator whose output precisely tracks the input voltage waveform. Two out of phase (by $\pi/2$) sine wave signals are derived (by 101,102) from the input sine wave (on 105), and these two out of phase signals are squared (in 115,117) and summed (in 119) to derive or estimate the desired square of the sine waveform signal at a fast response time while substantially excluding ripple of the estimated out of phase sine waves. An estimating circuit, described herein, comprises two integrator circuits (101,102) series connected into a substantially closed loop. The output of the second integrator (102) circuit is fed back to the input of the first integrator circuit (101). The output of each individual integrator circuit is a voltage sine wave separated in phase from the output of the other integrator by $\pi/2$ and in synchronism with the input substantially sine wave voltage $V_{AC}$. The output of each of the integrator circuits is squared in an associated squaring circuit (115,117). Each output of one of the two squaring circuits is summed (in 119) with the output of the other squaring circuit to produce the desired value of $V^2_{peak}$ or $V^2_{rms}$.

*FIG. 1*

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## Field of the Invention

This invention relates to signal estimation circuits and in particular to a signal sensing and estimation circuit for application to a power factor enhancement circuit included in a power supply circuit operating from an AC line supplying a sinusoidal or nearly sinusoidal voltage waveform.

## Background of the Invention

Power supplies operating directly off of an AC line typically comprise an input rectifier to convert the input AC line voltage to a DC voltage. This DC voltage is typically applied to a charge storage capacitor which is connected to the input of a DC/DC converter, which converts this DC voltage to a DC voltage of another level at its output. The operating characteristics of the rectifier and storage capacitor inherently distort the input current waveform at the input to the rectifier. This waveform distortion causes harmonics to be fed back onto the AC line and further leads to significant EMI emissions and to unnecessary power losses in the AC distribution circuitry.

In other applications power supplies may operate directly off of an AC line to drive a frequency changer to provide a signal at a different frequency from that on the AC line. The input waveform may be distorted leading to the difficulties described above.

The distortion of the input current waveform may be controlled by using an active power factor controller and a converter, such as a boost converter, inserted between the rectifier and the storage capacitor to actively control the input current waveform. The active switching device is controlled in response to a control circuit that monitors the input voltage waveform. The control modulates the conduction intervals at a high frequency compared with the AC line frequency, so that the wave form of the input current is constrained to conform to that of the input voltage waveform or to the fundamental sinusoidal waveform of that input voltage waveform.

Active power factor control networks typically sense input and output signal parameters of the power circuit and utilize a power switch selectively switched or pulse width modulated in response to these signal parameters to force the input current to conform to a desired current waveform. In a particular illustrative arrangement disclosed in U. S. patent 4,412,277 a rectified input voltage waveform is multiplied with an error voltage representing the deviation of the output voltage from a regulated value. The resulting control signal is properly scaled and used to control the modulating pulse driving the power switch to provide the desired input current waveform. In a more sophisticated power factor control arrangement disclosed in U. S. patent 4,677,366 a feedforward control is added to compensate for rapid change in the rms input AC voltage. This is used to inversely scale the programmed input current by the square of the rms input voltage.

A limitation with these existing arrangements is the effect of ripple existing in the sensed voltage waveforms which have undesirable effects in the operation of the control circuitry resulting in an inaccurate determination of the waveform of the programmed input current. At present techniques to deal with this ripple current lengthen the response time of the power factor correction circuitry resulting in substantial transient signals in the output voltage unless a large output charge storage capacitor is used.

The success of the controller in generating the correct current waveform is dependent on the speed and accuracy with which it derives or estimates the $V^2_{rms}$ or equivalently the $V^2_{peak}$ of the input voltage for use by the controller in controlling the boost converter's active power switch. This quantity has traditionally been derived by full-wave rectifying the input AC sine wave, filtering the rectified sine wave and squaring the filtered signal. While this technique has the advantage of simplicity of circuitry and of its inherent operation, it has the disadvantage of requiring a design trade off between ripple in the derived squared voltage and the speed with which the circuit can respond to dynamic changes in the input voltage.

## Summary of the Invention

An estimating circuit for application in estimating or deriving the value $V^2_{rms}$ or $V^2_{peak}$ of a line voltage $V_{AC}$ provides fast response time and a substantially ripple free value for these signals by the utilization of a controlled harmonic oscillator whose output tracks the fundamental of the input voltage waveform. Two out of phase (out of phase by $\pi/2$) sine wave signals are derived from the input sine wave.and these two out of phase signals are squared and summed to derive or estimate the desired square of the peak of the sine waveform signal with a fast response time.

The estimating circuit, according to an illustrative embodiment of the invention, comprises two integrators, with gain, series connected into a substantially closed loop. The output of the second integrator is summed with the sensed AC line sinusoidal waveform $V_{AC}$ and fed back to the input of at least one of the two integrators. The output of each individual integrator is a voltage sine wave separated in phase from the output of the other integrator by $\pi/2$ and in synchronism with the input substantially sine wave voltage $V_{AC}$. The output of each of the integrators is squared in an associated squaring circuit. Each output of one of the two squaring circuits is summed with the output of the other squaring circuit to produce the desired value of $V^2_{peak}$ or $V^2_{rms}$.

For rectifiers designed to operate in a particular

country, the AC line frequency, usually 50Hz or 60Hz, is known accurately and the estimating circuit described above operates with this a priori knowledge. However for estimating circuits designed to operate in applications with an uncertain line frequency without circuit adjustment, an adaptive feedback loop may be added to the estimating circuit, in accord with the invention, to accommodate different or varying line frequencies.

In accord with the invention this estimating circuit is included in the control of a power factor control system and is utilized to generate substantially ripple free estimates of control input parameters ($V^2_{peak}$ and signal frequency) and by the use of substantially ripple free signals controls a boost, buck, SEPIC or other related type converter to enhance the power factor at the input to a rectifier circuit powered directly off of an AC line. In addition the output of the integrator, whose output is in phase with the input AC voltage, can also be used as a control input signal, closely representative of the ideal AC input voltage waveform, for controlling the power factor controller to reduce input harmonics in order to reduce distortion of the input AC line voltage by the rectifier.

Functionally equivalent variations of this peak-squared estimating circuit may be designed by taking linear transformations of the process described above. For example, circuit variations can be readily designed in which the gains of the integrators are not equal, or the phases of the derived sinusoidal signals are not separated by $\pi/2$. To produce a ripple-free estimate of the square of the peak of the AC input voltage now requires a more generalized quadratic operation in which products of the signals are used as well as squares of the signals with unequal gains. These derived circuits nonetheless are functionally equivalent to the basic circuit described above.

Additionally, the process described above can be implemented with digital computation, or with a hybrid approach in which a combination of digital computation and analog circuitry is used.

## Brief Description of the Drawing

In the Drawing:

FIG. 1 is a functional schematic of an estimating circuit for determining a magnitude of a peak square value of an applied AC voltage and a signal closely representative of the ideal sinusoidal AC input voltage;

FIG. 2 is a functional schematic of an estimating circuit for determining a frequency of a fundamental sinusoid of an applied AC voltage in addition to the signals derived in the circuitry of FIG. 1;

FIG. 3 is a schematic of an illustrative estimating circuit embodied in a structure suitable for application to the power factor control rectifier circuits powered off of an AC line;

FIG. 4 is a schematic of an illustrative rectifier powered off of an AC line using such an estimating circuit in a power factor control circuit.

FIG. 5 is a schematic of an integrator which may be used in the circuit of FIG. 1 to accommodate two input line frequencies;

FIG. 6 is a schematic of circuitry for enabling the circuits used as the integrators in FIG. 1, to respond automatically to different frequency inputs; and

FIG. 7 is a schematic of an estimating circuit incorporating the circuitry of FIG. 6 to allow it to automatically select the gain of the integrators for different frequency inputs.

## Detailed Description

The estimating circuit of FIG. 1 includes first and second integrators 101 and 102 connected in series and within a substantially closed feedback loop 103 to form a controlled harmonic oscillator. The term "controlled harmonic oscillator" as used herein refers to an oscillator producing a sine wave oscillatory signal at a controlled amplitude and phase. A substantially sinusoidal AC voltage waveform is applied to the input terminal 105.

The two integrators 101 and 102 may comprise operational amplifiers connected as integrators with each having the gain $\omega$. The value for $\omega$ is determined by the angular frequency of the fundamental of the input sinusoidal AC voltage waveform. Each of these integrators 101 and 102 integrates the volt-second value of a sinusoidal waveform applied to its input. Equivalent circuits (i.e. digital, hybrid circuits etc) capable of integrating the volt-second value of an input voltage waveform may be used.

These integrators 101 and 102 are connected in cascade and hence the output of the integrator 102 is the integral of the sinusoidal input of the integrator 101 and hence in phase with the input sinusoidal voltage waveform applied to the input lead 105. The output of the integrator 102 is summed with the the AC sinusoidal voltage appled to the input lead 105

This output of the second integrator 102 signal is applied, with opposite sign, to the input of the first integrator 101 which forms the closed feedback loop of a controlled harmonic oscillator.

The input sinusoidal signal, on lead 105, and the output of integrator 102 is summed in a summing circuit 107 and the resultant sum is applied to two gain circuits 111 and 113. These gain circuits are included to permit the output of of the integrator 102 to track with a fast time response the amplitude and phase of the fundamental of the input AC voltage. The gain of the gain circuits 111 and 113 ("a" and "b") are selected to control the time response of the controlled harmon-

ic oscillator (e.g. the two series connected integrators 101 and 102 with feedback loop 103) by controlling the location of the estimator's (i.e. observer's) poles. Suitable values, for the illustrative embodiment, may be a=1 and b=0. These values are illustrative and may not be optimal for particular applications.

The output of the summing circuit 107 is applied with the gain b (assuming that "b" is a finite value other than zero) of gain circuit 111 to the summing circuit 109 where it is summed with the output of integrator 102 and the sum applied to the input of integrator 101. If "b" is equal to zero this is an open connection and no gain is applied to the integrator 102. The gain "b" might not be set to zero in order to adjust the form of the transient response of the controlled harmonic oscillator. An appropriate selection of values for the gains "a" and "b" will be apparent to those skilled in the art and need not be discussed herein in detail. The output of the integrator 101 is applied to the summing circuit 110 which sums it with the output of integrator 102 as amplified by the gain of the gain circuit 113. The output of the summing circuit is applied to the input of integrator 102.

The desired resultant signals occurring at the nodes 125 and 126 are two sinusoidal signals at the fundamental frequency and displaced in phase by $\pi/2$ from each other. These two sinusoidal signals at nodes 125 and 126 are applied to the squaring circuits 115 and 117 which provide the amplitude of the two sinusoidal signals as an algebraic squared value.

The outputs of the squaring circuits 115 and 117 are applied to the summing circuit 119, which produces a pure algebraic signal magnitude representing a square of the peak of the input sinusoid voltage waveform, applied to lead 105, on output lead 121. This output magnitude on output lead 121 represents the value $V^2_{peak}$ of the fundamental of the input voltage $V_{AC}$ without any significant imposed ripple. Derivation of this magnitude by the estimating circuitry is due to the trigonometric relation

$$COS^2(\theta) + SIN^2(\theta) = 1$$

for any value of $\theta$ which is functionally incorporated within the circuitry.

This circuit is extended in FIG. 2 to derive the fundamental frequency of the input $V_{AC}$ signal applied to the input lead 105. In this arrangement the outputs of the two squaring circuits 115 and 117 are connected, via leads 240 and 241, to an integrator 225. These outputs are combined in the integrator 225 which is designated as having the gain "d" selected to provide a long response time, typically one second or longer. This integration in conjunction with adjustment of the gains of the integrators 101 and 102 extracts the value of the fundamental frequency $\omega$ of the input $V_{AC}$ and supplies this value on the output lead 226. This value $\omega$ is fed back to the integrators 201 and 202 via lead 222.

The value of the gains "a" and "b" selected for the gain circuits 211 and 213 are selected, in the illustrative embodiment, to adjust the transient response time and transient characteristics of the controlled harmonic oscillator.

As shown an output lead 227 is provided to extract the value of the fundamental sine waveform ($\varepsilon \sin(\omega t)$) directly from the output of the integrator 202. This fundamental value is useful in some forms of control used in power factor enhancement.

An illustrative implementation of the peak estimating circuit of FIG. 1, using conventional analog circuit components, is shown schematically in the FIG. 3. The circuit of FIG. 3 includes the two operational amplifiers 301a and 302a each having the appropriate feedback circuitry to enable them to operate as the integrators 301 and 302 and further being interconnected with each other in a closed loop, by feedback loop 303, to form a controlled harmonic oscillator.

The sinusoidal line voltage is applied to the input terminals 305 and 335 and is coupled, via the operational amplifier 306, to the integrator 302, via a resistor network 307, which operates to sum this voltage with the output of the integrator 301, as applied to operational amplifier 302a of the integrator 302 via a resistor 307a which is part of the summing circuit 307. These resistors in combination with feedback circuit 302c of the operational amplifier 302a perform the desired summing and integration functions.

The circuit includes two commercially available multiplier chips 315 and 317, (e.g. MC 1495) which are externally connected to multiply an applied signal with itself and hence square it. Specifics of this connection are dictated by the multiplier chip data sheet and are not herein discussed. The multipler chip 315 is responsive to the output of the integrator 301 supplied to it via lead 335. The multiplier chip 317 receives its input from the integrator 302, via lead 337 from the integrator 302. The output of the multiplier chips 315 and 317 are coupled via the leads 345 and 347 to the summing circuit 319 (e.g an operational amplifier connected to sum two inputs) which supplies the desired peak squared value of the fundamental of the input sinusoidal input voltage on output lead 321.

Application of the estimating circuit of FIG. 1 is shown in schematic form in the FIG. 4 which shows a representative power factor enhancement system. The power factor enhancement system includes a rectifier 403, a boost converter 405 and a control circuit 417 responsive to the input from an estimator such as is shown in the FIGS. 1 or 2. The input AC voltage is applied to the input terminals 401 and 402 and full wave rectified by the rectifier 403. The rectified signal is applied to the boost converter which includes an inductor 406, a controlled power switch 407, a rectifying diode 408 and a charge storage capacitor 409.

The power switch is activated under control of a control circuit 417 to pulse width modulate the rectified sine wave so that the input current waveform is constrained to track the fundamental sine wave of the input AC voltage applied to the input terminals 401 and 402. The sine wave current is applied to the storage capacitor 409 and the output terminals 431 and 432.

The input AC voltage is sensed by the estimator 414, via the sensing leads 411 and 412. The estimator 414 derives a peak squared voltage on lead 421 and optimally a fundamental sine wave signal on lead 422 in the manner described above. The output voltage of the boost convert 405 is also applied to the control circuit via lead 418. These three input signals enable the control circuit to pulse width modulate the power switch 407 of the boost converter 405 to generate the desired current waveform.

The estimators disclosed above are designed for operation at a specific frequency of the input AC signal. It may be desirable, however, to provide for operation at differing frequencies with a single circuit pack.

For rectifiers which may be used in either 50Hz or 60Hz applications, the gains of the intergrators 201 and 202 in FIG. 2 need only be selectively set to gains of $2\pi 50$ or $2\pi 60$ respectively. A representative integrator having a step adjustable gain to provide the two gains of $2\pi 50$ and $2\pi 60$ is shown in the FIG. 5. Two series connected input resistors 522 and 523 to the integrator 510 are set to provide the needed gain for a particular frequency of operation. This gain is enabled as a selectable gain for the integrator circuitry 510, in FIG. 5, by using a switch 521 which shorts an input resistor 522. The switch 521 is opened for 50Hz operation, and closed for 60Hz operation.

The switch 521 is implemented, in the illustrative embodiment, by two series-connected but oppositely poled FETs 601 and 602 as shown in FIG. 6. FIG. 6 shows a representative controller to replace the integrator 225 shown in FIG. 2. It operates in response to the outputs 131 and 132 of the squarers 115 and 117 shown in FIG. 1 to control the gates of FETs 601 and 602. An operational amplifier 605 provides the desired gain $R_{2a}/R_{1a} = R_{2b}/R_{1b}$ to provide an output voltage on lead 620 which is representative of the frequency error of the estimating circuit of FIG. 1 with respect to the input frequency of $E_m \sin(\omega t)$. A typical gain for operational amplifier 605 would be minus one volt per hertz. If switches 601 and 602 are open for 50Hz operation and if a 60Hz input voltage waveform is applied to the estimator, then a -10V output appears on lead 620 from operational amplifier 605. Capacitors 622 and 623 in .6 may be selected to provide a response time of one second or more, taking advantage of the fact that the input frequency rarely is suddenly changed.

The operation of the circuit in FIG. 6 can be described as follows. If the estimator on FIG. 1 has been operating at 50Hz, then the voltage of lead 621 is approximately -15 volts and the voltage on lead 620 is near zero. The voltage on lead 622 is -5 volts as determined by the ratio of the resistor divider 640 and 641. Switches 601 and 602 are both open (i.e. the FETs are nonconducting).

If the AC input frequency changes to 60Hz, then the voltage from squarer 117 (i.e. lead 132) is smaller than that from 115 (i.e. lead 131), and the voltage on lead 620 falls to -10 volts. This voltage represents a +10Hz frequency error. The comparator 607 switches its output voltage on lead 621 to +15 volts, closing switches 601 and 602 (i.e. the FETs are conducting), and the voltage on lead 620 returns to nearly zero. The voltage on lead 622 is +5 volts, maintaining the comparator 607's output voltage, on lead 621, at +15 volts.

More elaborate circuits controlling the gains of integrators 201 and 202 to accommodate continuously varying input frequencies can be developed for use in conjunction with the circuit on FIG. 2 by adjusting the gains of the integrators 201 and 202 using either multiplying digital-to-analog converters or fully analog multipliers such as those based on Gilbert multiplier cells. Microprocessor controllers can also be used to provide an effective way to implement controllers with continuously variable input frequencies.

An illustrative estimator fully capable of operating in 50Hz and 60Hz environments is shown in the schematic of FIG. 7. The estimating circuit is essentially the circuit of FIG. 1 which has been modified by the circuitry of FIG. 6. Its operation is evident from the discussion above describing the schematics of FIG. 1 and 6. It includes the outputs 721 to provide the peak squared voltage and the output 727 to provide a sine wave voltage at the fundamental frequency.

## Claims

1. An estimating circuit for deriving a squared signal value from a substantially sinusoidal waveform signal;

   CHARACTERIZED BY:

   first and second integrators (101,102) series connected with each other in a substantially closed loop with an output of the first integrator coupled to an input of the second integrator and an output of the second integrator coupled to an input of the first integrator;

   an summing circuit (107) including an input for accepting the substantially sinusoidal waveform signal and a second input connected to receive an output of the second integrator;

   means for coupling an output of the first summing circuit into the closed feedback loop connecting to the second integrator;

   a first and second signal level squaring cir-

cuit (115,117) connected to square the signal output of the first and second integrator, respectively; and

a second summing circuit (119) for combining the signal outputs of the first and second signal level squaring circuits and an output (121) for supplying a squared value of the input substantially sinusoidal waveform signal.

2. An estimating circuit for deriving a squared signal value from a substantially sinusoidal waveform signal; as claimed in claim 1 and further comprising;

first means (111,109) for inserting gain in the means for coupling an output of the first summing circuit into the closed loop between the first and second integrator at an input to the first integrator;

second means (113,110) for inserting gain in the means for coupling an output of the first summing circuit into the closed loop between the first and second integrator at an input to the second integrator.

3. An estimating circuit for deriving a squared signal from a substantially sinusoidal waveform signal; as claimed in claim 2, and further comprising:

the first and second means for inserting gain including a gain source (111,113) and a summing circuit (109,110) connected within the feedback loop.

4. A method of estimating a peak signal value from a substantially sinusoidal waveform signal;

CHARACTERIZED BY the steps of:

integrating the sinusoidal waveform signal to generate a first integral value;

integrating the first integral value to generate a second integral value;

squaring the first integral value to generate a first squared value;

squaring the second integral value to generate a second squared value;

summing the first squared value with the second squared value to generate a non-periodic magnitude representative of the substantially sinusoidal waveform signal.

5. A method of estimating a peak signal value from a substantially sinusoidal waveform signal as claimed in claim 4; further comprising the steps of:

amplifying the substantially sinusoidal waveform signal with controlled gain preceding its first integration step.

6. A method of estimating a peak signal value from a substantially sinusoidal waveform signal as claimed in claim 5; further comprising the steps of:

combining and integrating the first and second squared values to generate a value representative of a fundamental frequency of the substantially sinusoidal waveform signal.

7. A method of estimating a peak signal value from a substantially sinusoidal waveform signal as claimed in claim 6; further comprising;

the step of amplifying includes selecting the gain for inserting with a value selected for controlling a desirable circuit admittance of an active power factor enhancing circuit with which the estimating circuit is to cooperate.

FIG. 1

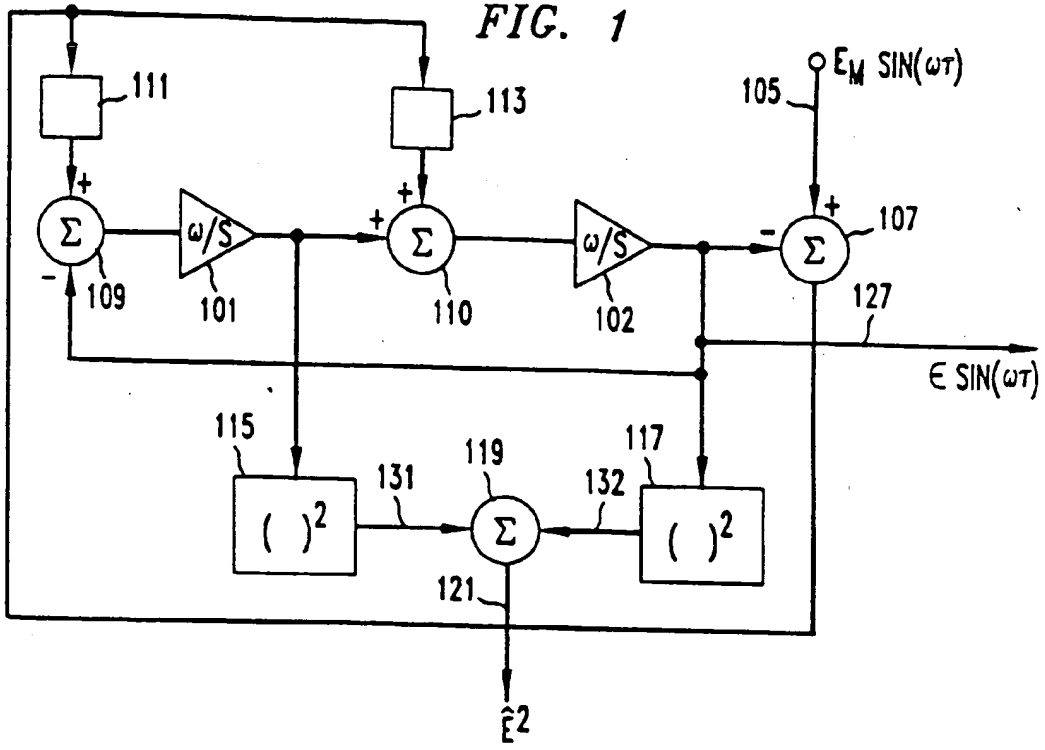
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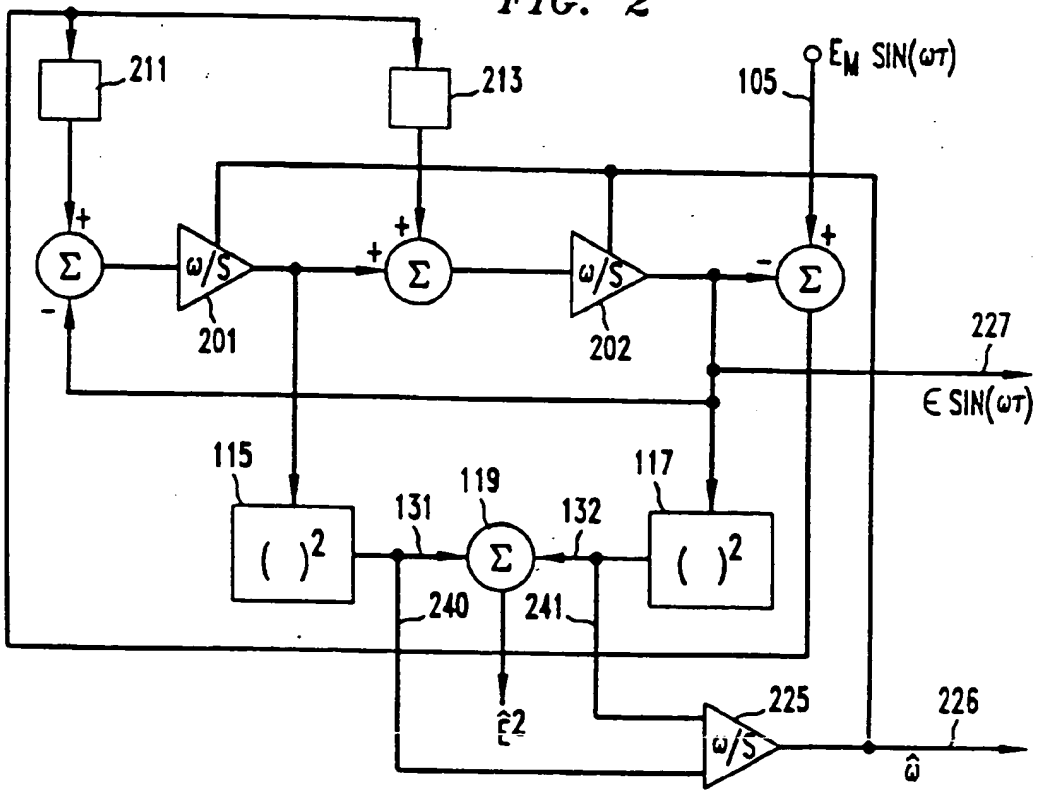
FIG. 2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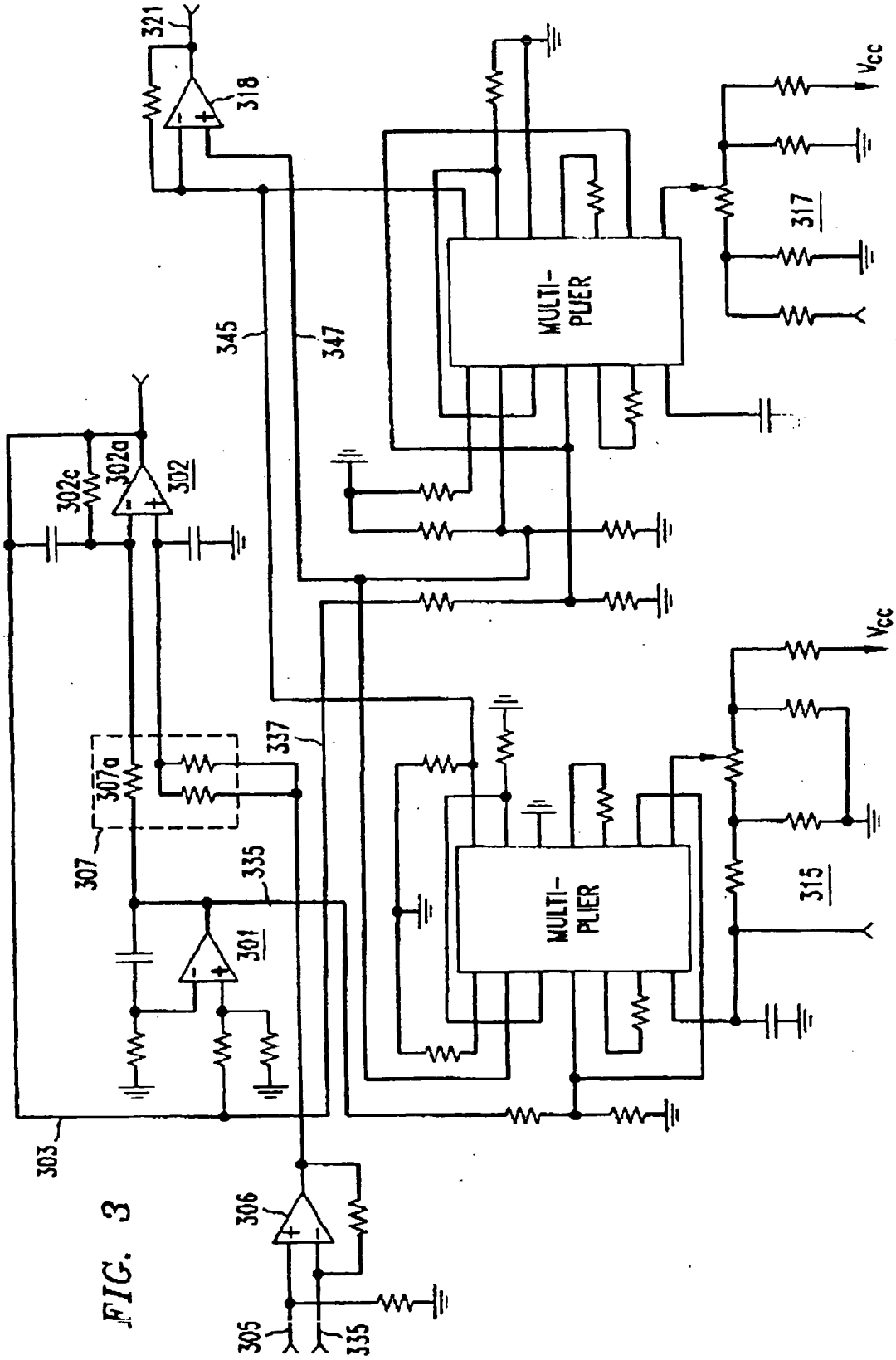
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305

FIG. 3

FIG. 4

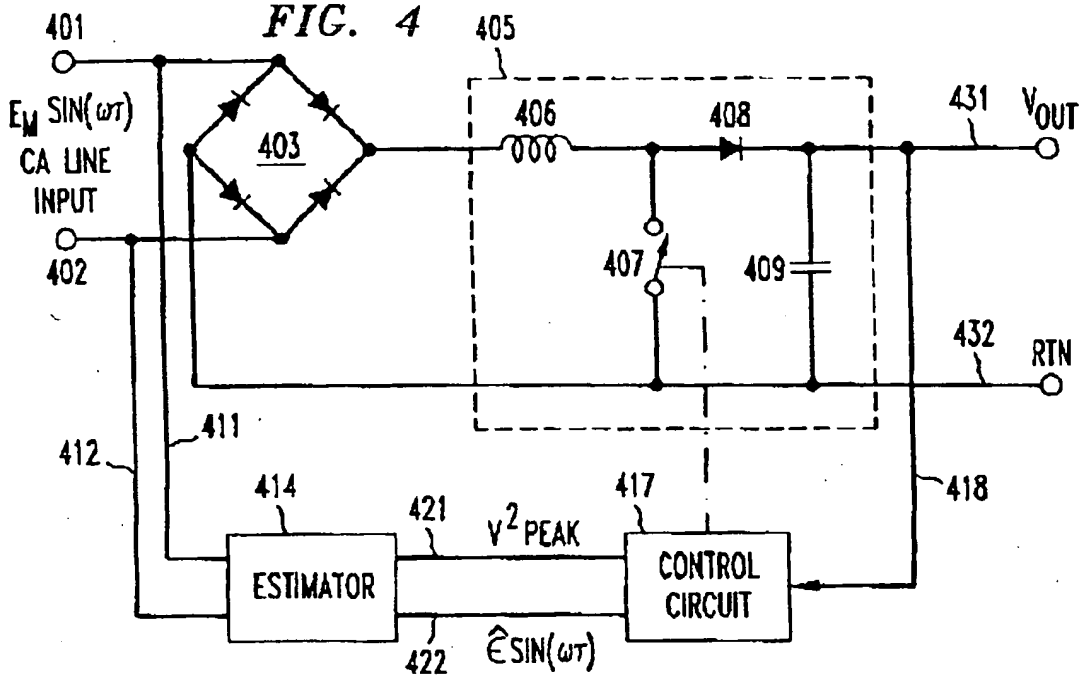



FIG. 5

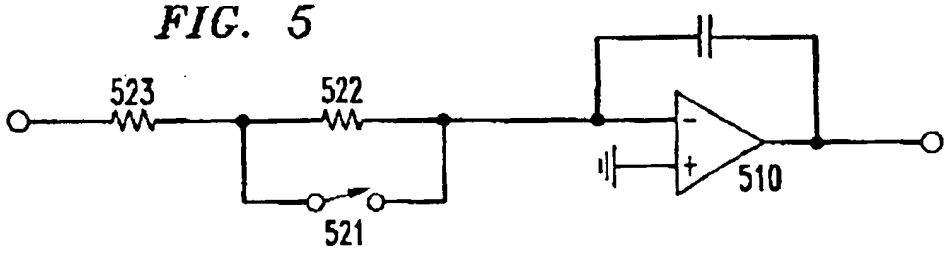



FIG. 6

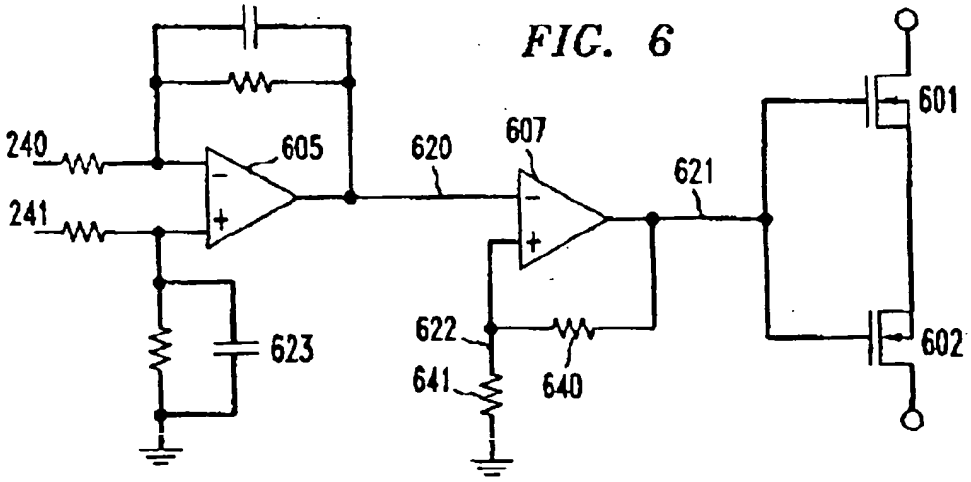
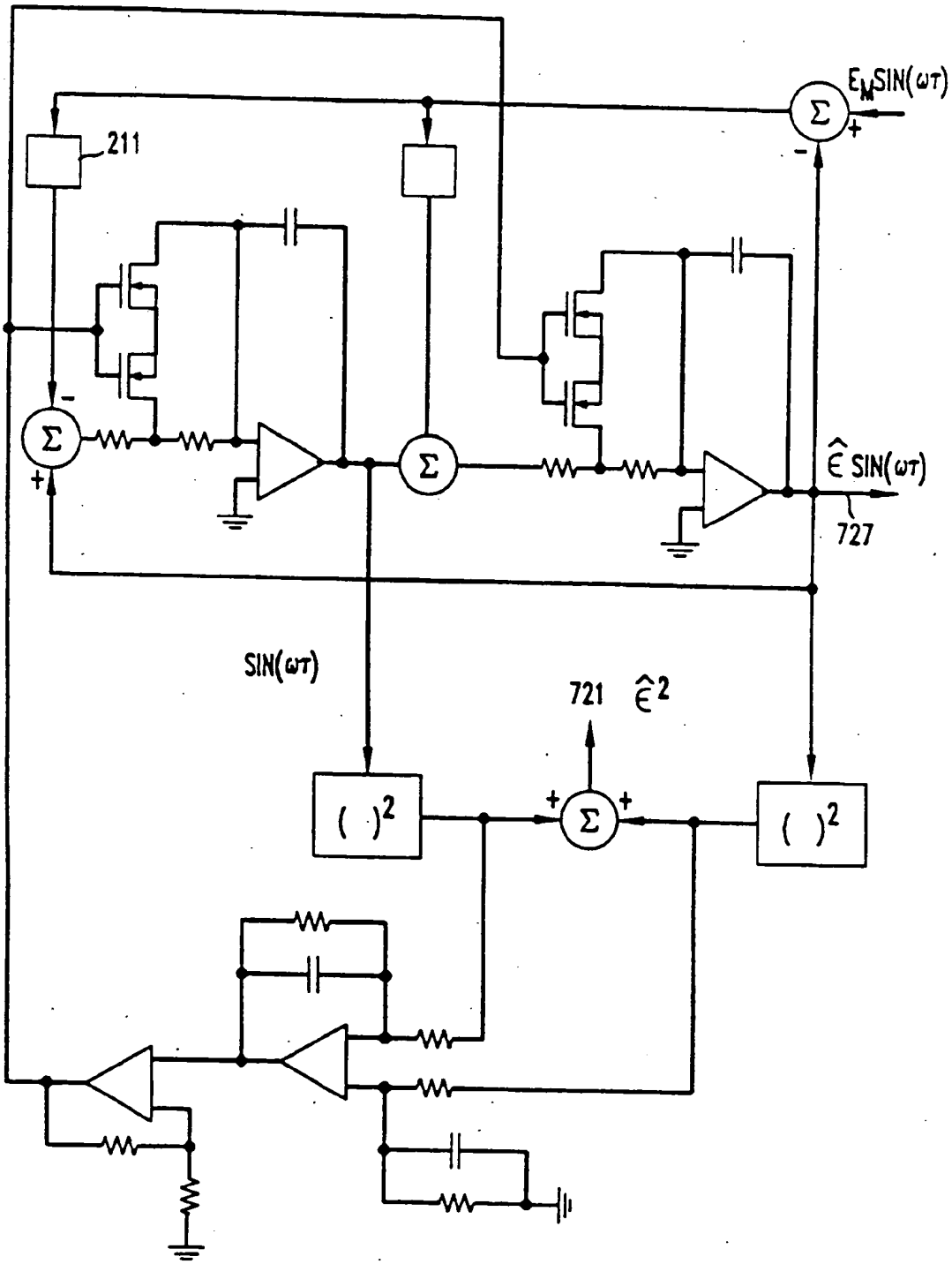


*FIG. 7*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( )²
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